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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/535,233	03/24/2000	Masaya Kadono	SEL 171	1670

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EXAMINER	
COLEMAN, WILLIAM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/535,233	KADONO ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *1-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0405*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 11-8, 23-32 and 34-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Kern, "Handbook of Semiconductor Wafer Cleaning Technology", Science, Technology and Applications, Noyes Publication, Westwood, New Jersey, USA 1993, pp. 1-151, 274-339 and 433-496.

3. Kern discloses a semiconductor process as claimed.

Pertaining to claim 1, Kern teaches a method of manufacturing a semiconductor device, comprising steps of:

forming a semiconductor film (i.e., device surface as disclosed on pp. 3, which is distinct from the wafer surface) formed over a substrate;

spinning the substrate (see **FIG. 7**, where motor/motor shaft spins multi-position turntable around on-center spray-post);

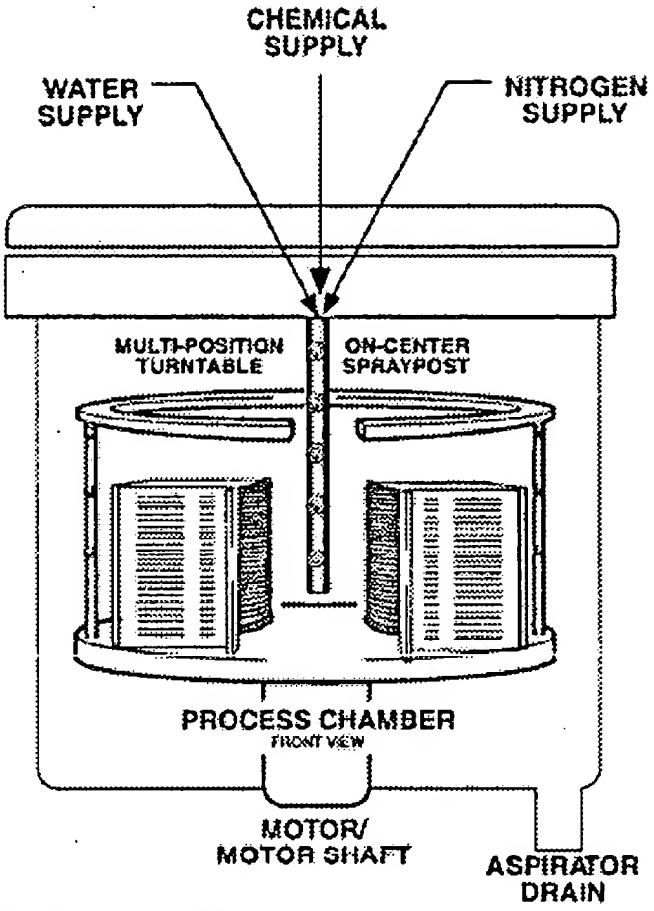

Figure 7. Multiposition spray processor.

applying an etching solution to a surface of said semiconductor film and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface by the step of applying the etching solution; and then

forming a gate insulating film in contact with said semiconductor film from the surface of which the contaminating impurity has been removed (the Examiner takes the position that since Kern teaches fabricating DRAM devices of ULSI silicon circuits, it is well known that DRAM devices require gate insulators as part of the fabrication scheme).

4. Pertaining to claim 12, Kern teaches a method according to claim 11, wherein the contaminating impurity is at least one element selected from periodic table group 1 elements or periodic table group 2 elements (page 9).

5. Pertaining to claim 13, Kern teaches a method according to claim 11, wherein the contaminating impurity element is at least one element selected from the group consisting of Na, K, Mg. Ca and Ba (page 9).

6. Pertaining to claim 14, Kern teaches a method according to claim 11, wherein the contaminating impurity is removed by an acidic solution containing fluorine (table 5, pp. 126)

Table 5. The Effect of HCl Addition into an HF Oxide Stripping Solution on Metallic Contamination on Silicon Wafer Surfaces (42)

Stripping Solution	SIMS Relative Element Concentration					
	Na	K	Al	Ca	Mg	Fe
10% HF	6	10	7	60	8	7
10% HF + HCl*	1	10	1	10	4	2

* Concentration not defined in reference.

7. Pertaining to claim 15, Kern teaches a method of manufacturing a semiconductor device, comprising steps of:

forming at least one semiconductor island over a substrate (please see FIG. 29, on pp 483).

spinning the substrate (as disclosed in the rejection of claim 11);

applying an etching solution to a surface of said semiconductor island and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface by the step of applying the etching solution; and then

forming a gate insulating film over said semiconductor island after the contaminating impurities are removed from the surfaces (please note that the Examiner takes since Kern teaches fabricating DRAM devices, this limitation has been met).

8. Pertaining to claim 16, Kern teaches a method according to claim 15, wherein said etching solution is selected from the group consisting of hydrofluoric acid, dilute hydrofluoric acid, ammonium fluoride, buffered hydrofluoric acid (BHF, hydrofluoric acid and aqueous hydrogen peroxide (FPM), and a solution mixture including ammonium hydrofluoride (NH_4HF_2) and ammonium fluoride (NH_4F) (LAL500).

9. Pertaining to claim 17, Kern teaches a method according to claim 15, wherein the contaminating impurity is at least one element selected from periodic table group I elements or periodic table group II elements (please see the rejection of claim 13 above).

Pertaining to claim 18, Kern teaches a method according to claim 15, wherein the contaminating impurity element is at least one element selected from the group consisting of Na, K, Mg, Ca, and Ba.

10. Pertaining to claims 23 and 27, Kern teaches a method of manufacturing a semiconductor device, comprising steps of:

forming a gate wiring over a substrate;

spinning the substrate;

applying an etching solution to surfaces of said substrate and said gate wiring and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surfaces by the step of applying the etching solution; and then

forming a gate insulating film and a semiconductor film over said gate wiring after the contaminating impurities are removed from the surfaces (the Examiner takes the position that since Kern teaches the fabrication of various semiconductor devices, the wiring layer is inherent).

11. Pertaining to claims 24, 28 and 31, Kern teaches a method according to claims 11, 23 and 27, wherein said etching solution is selected from the group consisting of hydrofluoric acid, dilute hydrofluoric acid, ammonium fluoride, buffered hydrofluoric acid (BHF, hydrofluoric acid and aqueous hydrogen peroxide (FPM), and a solution mixture including ammonium hydrofluoride (NH_4HF_2) and ammonium fluoride (NH_4F) (LAL500).

12. Pertaining to claim 25 and 29, Kern teaches a method according to claims 23 and 27, wherein the contaminating impurity is at least one element selected from periodic table group I elements or periodic table group II elements.

13. Pertaining to claims 26 and 30, Kern teaches a method according to claims 23 and 27, wherein the contaminating impurity element is at least one element selected from the group consisting of Na, K, Mg, Ca, and Ba..

14. Pertaining to claims 33, 34 and 35, Kern teaches a method according to claims 15, 23 and 27, wherein the contaminating impurity is removed by an acidic solution containing fluorine (see 5.1 pp. 310).

15. Claims 19-22 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Chiyou et al., Patent Abstracts of Japan 11-016866.

Chiyou discloses a semiconductor process as claimed.

16. Pertaining to claim 19, Chiyou teaches a method of manufacturing a semiconductor device, comprising steps of:

forming a semiconductor film **3** formed over a substrate **1**;

crystallizing said semiconductor film [0052]

spinning the substrate [0051];

forming at least one semiconductor island over said substrate by patterning the crystallized semiconductor film [see Drawing 3];

applying an etching solution to a surface of said semiconductor film and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface; and then forming a gate insulating film over said semiconductor island after the contaminating impurities are removed from the surfaces by the step of applying the etching solution; and

forming a gate electrode over said gate insulating film (please note that since Chiyou teaches DRAM, EPROM, MPU and switching transistor and a liquid crystal display the gate electrode and gate insulating layer is well known to be incorporated in the above devices).

17. Pertaining to claim 20, Chiyou teaches a method according to claim 19, wherein said etching solution is selected from the group consisting of hydrofluoric acid, dilute hydrofluoric acid, ammonium fluoride, buffered hydrofluoric acid (BHF), hydrofluoric acid and aqueous hydrogen peroxide (FPM), and a solution mixture including ammonium hydrofluoride (NH_4HF_4) and ammonium fluoride (NH_4F) (LAL500).

18. Pertaining to claim 21, Chiyou teaches a method according to claim 19, wherein the contaminating impurity is at least one element selected from periodic table group I elements or periodic table group II elements (the Examiner takes the position that it is well known that metal ions from the group I and group II elements of the periodic table as conventional contaminants for the silicon process).

19. Pertaining to claim 22, Chiyou teaches a method according to claim 19, wherein the contaminating impurity element is at least one element selected from the group consisting of Na, K, Mg, Ca and Ba (the examiner takes the position that the claimed elements are one of the major sources of contaminants).

20. Pertaining to claim 36, Chiyou teaches a method according to claim 19, wherein the step of crystallization is performed by irradiating a laser light [0046].

Response to Arguments

21. Applicant's arguments filed April 4, 2005 have been fully considered but they are not persuasive.

22. Applicants contend that Kern, "Handbook of Semiconductor Wafer Cleaning Technology, Science, Technology and Applications" Noyes Publications, 1993, herein known as Kern fails to teach steps (1)-(3), which are (1) forming a gate insulating film in contact with the semiconductor film having a surface from which the contaminating impurity has been removed (claims 11 and 15); (2) forming a gate wiring over a substrate; and (3) forming a gate insulating

film and a semiconductor film over the gate wiring after the contaminating impurities are removed from the surface, because there is no clear teaching of the above steps.

23. In response to Applicants contention that Kern fails to teach forming a gate insulating film in contact with the semiconductor film having a surface from which the contaminating impurity has been removed, Applicants are directed starting at page 3 which discusses the importance of cleaning wafer surfaces in the fabrication of semiconductor microelectronic devices. Kern further discloses that it is well known that the device performance, reliability, and product yield of silicon circuits are critically affected by the presence of chemical contaminants and particulate impurities on the wafer or device surface. The Examiner takes the position that the device is fabricated on the surface of the wafer and Kern is concerned about the cleanliness of both the wafer surface and the device surface. It is also well known that the device surface is a build up of different materials, for instance forming and patterning an oxide on a semiconductor surface to make MOS devices. It is also well known that DRAM devices are MOS devices and these devices or structures sit above the surface of the wafer. Kern further explains that hundreds of processing steps in the fabrication of advanced silicon circuits can contribute to contamination (see pp 11). Removing unwanted impurities would imply the concept of cleaning and since there are hundreds of processing steps I the fabrication of advanced silicon circuits, this will imply hundreds of cleaning steps to minimize contamination.

24. It appears that Applicants are implying that the Dynamic Random Access Memory devices (DRAM) discussed by Kern would not have the features of gate insulating films nor gate wirings as claimed, the Examiner has provided several references in which these features are

disclosed. Applicants are also implying that DRAMS would not appear as island features on a semiconductor wafer, this argument is also moot as disclosed what is well known in the industry.

25. Applicants contend that Chiyou et al., Japanese Patent Abstracts Publication 11-016866 fails to teach forming a gate insulating film over said semiconductor island.

26. In response to Applicants contention that Chiyou fail to teach forming a gate insulating film over said semiconductor island, Applicants are directed to drawings 1-4 and paragraphs 0002 and 0046. In paragraph 0002, Chiyou discloses fabricating various semiconductor devices and in paragraph 0046, Chiyou teaches a glass substrate with an amorphous silicon film above it. It is well known that a plurality of devices are formed on substrates and islands will inherently be formed. Therefore a DRAM formed on a glass substrate will inherently have a gate insulating film over a semiconductor island. Therefore Applicants arguments are moot.

Conclusion

27. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

28. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on 9:00 AM-5:00 PM.

30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC